UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/816,269 | 03/31/2004 | Robert P. Masleid | TRAN-P293 | 9824 |

7590 04/17/2007

WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

| EXAMINER | |
|---|---|
| PHAM, LONG | |
| ART UNIT | PAPER NUMBER |
| 2814 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 04/17/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/816,269 | MASLEID ET AL. | |
| | Examiner | Art Unit | |
| | Long Pham | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2,6-12,16-22 and 26-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 6-12, 16-22, 26-33, and 34-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 recites the limitation "said semiconductor" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 11 recites the limitation "said semiconductor" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 21 recites the limitation "said semiconductor" in line 4. There is insufficient antecedent basis for this limitation in the claim.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 6-12, 16-22, 26-33, and 34-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (US publication 2001/0024859).

With respect to claims 1 and 21, Takahashi et al. teach a semiconductor device having a surface, comprising (see all disclosed figures, specifically figs. 19(a)-19(b), 20(a)-20(b), and 49 and associated text):

A plurality of conductive sub-surface regions 22nb, 23nb, etc. of a first conductivity each formed beneath said surface **of said semiconductor device**, wherein said conductive sub-surface regions form a sub-surface structure and said sub-surface structure has a perimeter (fig. 49);

An isolation structure SGI formed within said perimeter of said sub-surface structure such that said isolation structure creates a gap or separation in said sub-surface structure; and

At least one metal structure L1 formed above said surface, wherein said metal structure spans or runs over said gap and is coupled to said sub-surface structure via a plurality of tap contacts CON1.

Further with respect to claims 1 and 21, Takahashi et al. teach the conductive sub-surface regions as claimed, it is capable of routing a body-bias voltage.

With respect to claim 11,

Takahashi et al. teach a semiconductor device having a surface, comprising (see all disclosed figures, specifically figs. 19(a)-19(b), 20(a)-20(b), and 49 and associated text):

A first plurality of conductive sub-surface regions 22nb,etc. of a first conductivity each formed beneath said surface **of said semiconductor device**, wherein said conductive sub-surface regions form a first sub-surface structure and said sub-surface structure has a perimeter (fig. 49);

A second plurality of conductive sub-surface regions 23nb of said first conductivity each formed beneath said surface, wherein said second plurality of conductive sub-surface regions form a second sub-surface structure;

An isolation structure SGI formed between said first sub-surface structure and said second sub-surface structure such that said isolation structure creates a gap or separation between said first sub-surface structure and said second sub-surface structure; and

At least one metal structure L1 formed above said surface, wherein said metal structure spans or runs over said gap and is coupled to said first sub-surface structure and said second sub-surface structure via a plurality of tap contacts CON1.

**Further with respect to claims 1, 11, and 21, Takahashi et al. further teach each of the conductive sub-surface regions 22nb, 23nb, etc is buried at a depth below said surface (wherein the surface of the semiconductor device is being interpreted as any surface (eg. a surface of a gate) and not limited to the surface of substrate and "buried" is being interpeted as buried in the semiconductor device and not limited to "buried in the substrate".**

With respect to claim 12, Takahashi et al. further teach the first sub-surface structure is a first diagonal sub-surface mesh structure, and wherein said second sub-surface structure is a second diagonal sub-surface mesh structure. See figs. 19(a) and 20(a).

With respect to claims 2 and 22, Takahashi et al. further teach the sub-surface structure is a diagnoal sub-surface mesh structure. See figs. 19(a) and 20(a).

With respect to claims 6, 7, 16, 17 26, and 27, Takahashi et al. further teach each conductive sub-surface region has an N-type or P-type doping. See fig. 49.

With respect to claims 8, 18, 28, Takahashi et al. further teach each conductive sub-surface region has a strip shape. See fig. 49.

**With respect to claims 9 and 19, Takahashi et al. further teach the metal structure is metal wire shape. See fig. 49 and paragraph [0206].**

**With respect to claim 29, col. 1, lines 45-55 of US patent 5,554,554 discloses that the use of polysilicon interconnection is well-known.**

**With respect to claim 31, col. 1, lines 25-35 of US patent 4,443,295 discloses that the use of polysilicon interconnection is well-known.**

**With respect to claim 30, the doping of the polysilicon interconnection to increase its conductivity is well-known.**

With respect to claims 10, 20, 32, Takahashi et al. further teach a plurality of second conductive sub-surface regions 23nb of said first conductivity each formed under each portion of said metal structure that overlaps said sub-surface structure, wherein each second conductive sub-surface region has a continuous sub-surface layer shape. See fig. 49.

With respect to claim 33, Takahashi et al. further teach the isolation structure divides the sub-surface into a first portion and a second portion. See fig. 49.

**With respect to claim 34, Takahashi et al. further teach that the plurality of conductive sub-surface regions inherently form a conductive path and the conductive path would inherently be capable of routing the body-bias voltage. Further, how the plurality of conductive sub-surface regions are selected has not been given patentable weight since claims are directed to a structure.**

**With respect to claims 35, 40, and 45, Takahashi et al. further teach that the plurality of conductive sub-surface regions would inherently prevent the isolation of wells (PWp1, NWp1, PWp2, NWp, etc) 2of the semiconductor device since they provide conductive path. See figure 49.**

**With respect to claims 36, 41, and 46, Takahashi et al. further teach that the plurality of conductive sub-surface regions have a pattern, a location, and size and wells inherent have distributions. Furhter, how the pattern, location, and size are selected has not been given patentable weight since claims are directed to a structure. See figure 49.**

**With respect to claims 37, 42, and 47, Takahashi et al. further teach that the isolation structure SGI creates a gap that separates the conductive sub-surface regions to at least two regions. See figure 49.**

**With respect to claims 38, 43, and 48, Takahashi et al. further teach that the isolation structure SGI creates a gap that interrupts the conductive sub-surface regions to at least two regions. See figure 49.**

**With respect to claims 39 and 44, Takahashi et al. further teach that the first and second plurality of conductive sub-surface regions inherently form a conductive path and the conductive path would inherently be capable of routing the body-bias voltage. Further, how the plurality of conductive sub-surface regions are selected has not been given patentable weight since claims are directed to a structure.**

***Response to Arguments***

Applicant's arguments with respect to claims 1-2, 6-12, 16-22, 26-33, and 34-48 have been considered but are moot in view of the new ground(s) of rejection.

In response to the applicant's arguments in the the paragraph bridging pages 13 and 14 of the amendment dated 01/24/07, it is submitted that a surface of the gate constitutes a surface of the semiconductor device, and the plurality of conductive sub-surface regions 22nb, 23nb, etc are formed beneath the surface of the gate or the surface of the semiconductor device.

In response to the applicant's arguments in the first and second full paragraphs on page 14 of the amendment dated 01/24/07, see the attached copy of examiner's explanation and interpretation of fig. 49 of Takahashi et al.

In response to the applicant's arguments in the paragraphs on page 15 of the amendment dated 01/24/07, it is submitted that since Takahashi et al. teach the claimed structure, it is capable of be used for routing of a body-bias voltage.

In response to the applicant's arguments in the the paragraph bridging pages 16 and 17 and the first full paragraph on page 17 of the amendment dated 01/24/07, see the attached copy of examiner's explanation and interpretation of figs 19(a) and 20(a) of Takahashi et al.

In response to the applicant's arguments in the paragraph at the bottom of page 14 of the amendment dated 01/24/07, it is submitted that Takahashi et al. further teach a plurality of second conductive sub-surface regions 23nb of said first conductivity each formed under each portion of said metal structure that overlaps said sub-surface structure, wherein each second conductive sub-surface region has a continuous sub-surface layer shape. See fig. 49.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

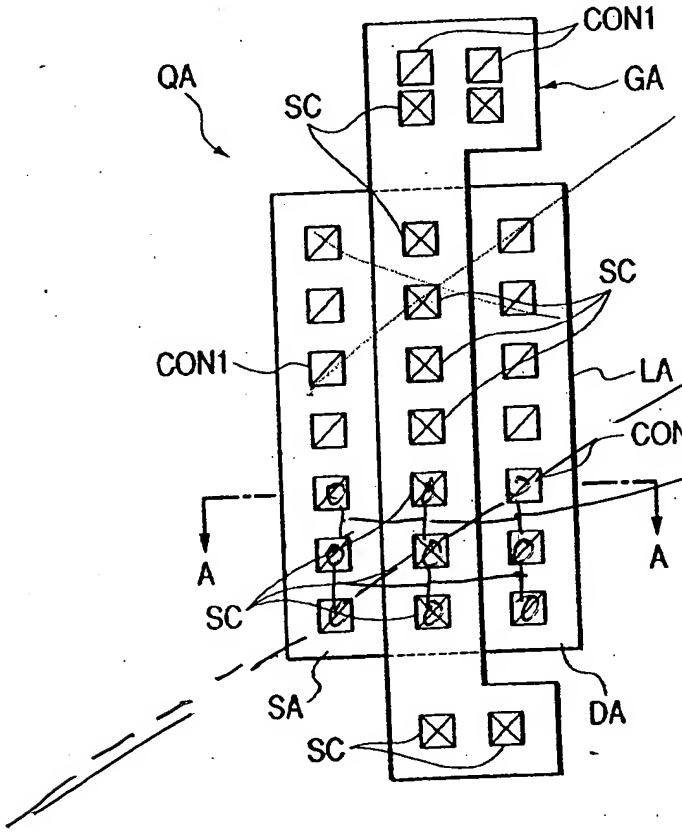
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

LP

FIG. 19(a)




diagonal structure

areas under these contacts are sub-surface regions and these sub-surface regions form a diagonal sub-surface

FIG. 19(b)

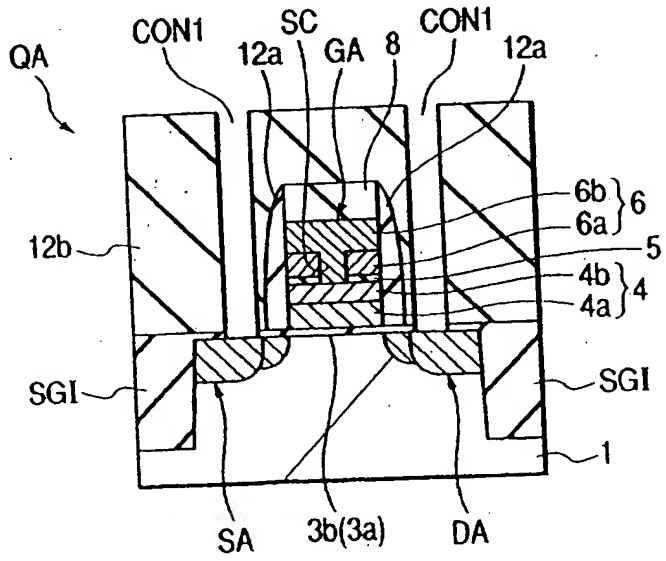


FIG. 20(a)

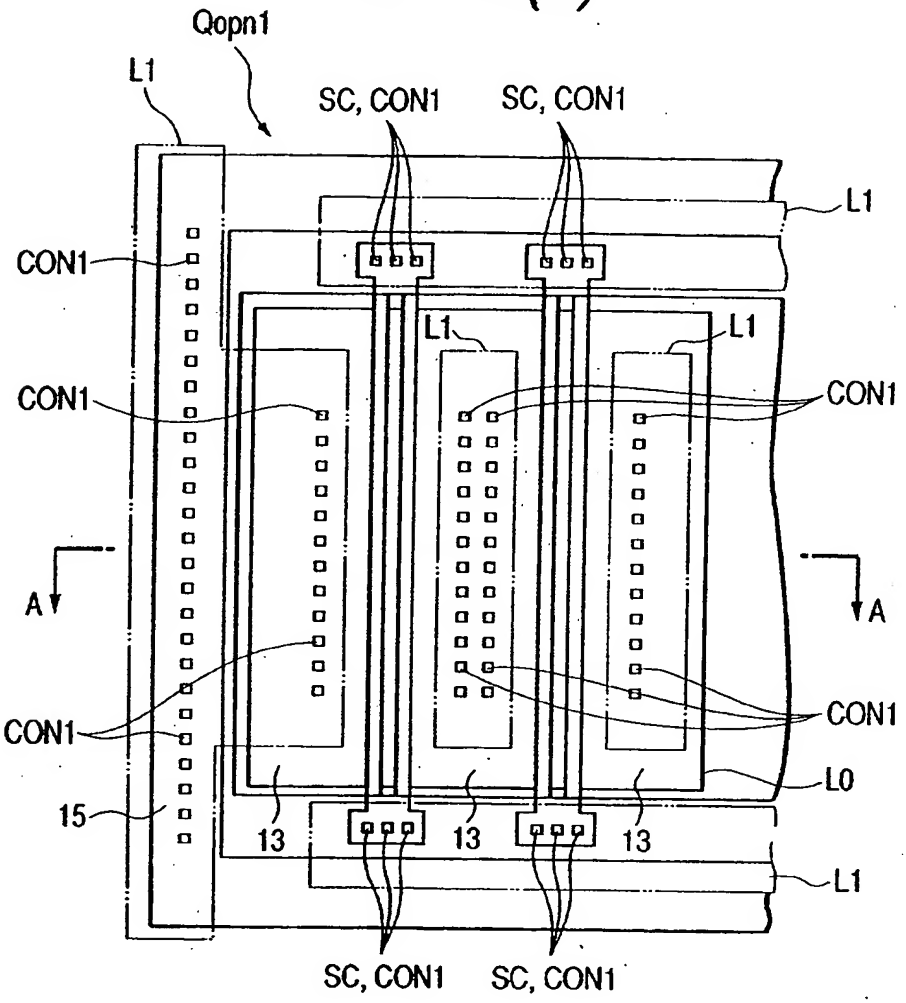



FIG. 20(b)

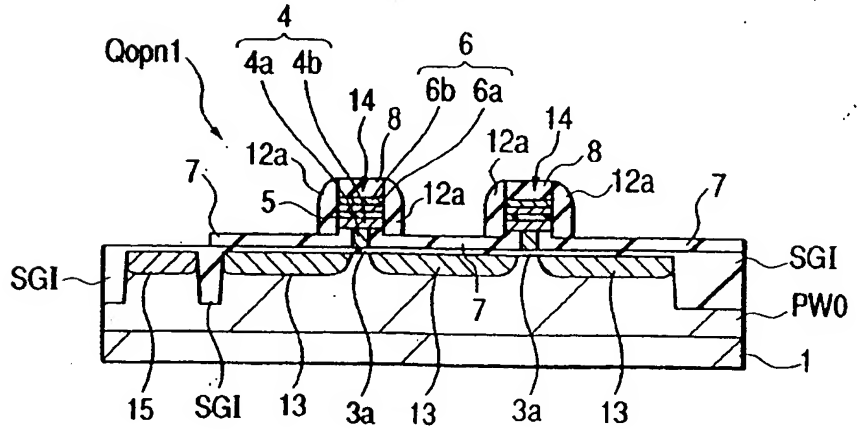


FIG. 49